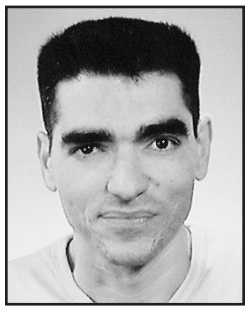
Session 26 Overview

Non-Volatile Memories



Chair: Hideto Hidaka, *Renesas Technology, Itami, Japan*

Associate Chair: Yair Sofer, *Saifun Semiconductors, Netanya, Israel*

A wide range of applications is emerging to take advantage of diverse non-volatile memory technologies. From stringent automotive applications demanding reliability in high temperatures to ultra-low-power computing in handheld consumer devices, the forefront of non-volatile memory is advancing in density, speed and a variety of features. RFID-tag applications require ultra-low-power non-volatile memory and a very small form factor. To meet the expanding needs of application requirements, this session presents advancements in phase-change RAM (PRAM), magnetic RAM (MRAM), NOR type flash memories and an electron-beam-written ROM.

Paper 26.1 from Samsung starts the session with a breakthrough, reporting the first published 512Mb PRAM using a diode-switch storage cell in 90nm technology and featuring 266MB/s read and throughput.

Paper 26.2 from Hitachi and Renesas describes a different implementation of phase-change memory for embedded applications. Using with a 100μA write-current cell structure, this ultra-low-power design operates with a 1.5V supply, and opens a new era for easy-to-use logic-compatible applications.

In the NOR flash memory arena, Paper 26.3 from STM introduces the first gigabit-level integration in 65nm technology with 2 bits per cell. This first implementation of a DDR interface for NOR flash provides 400MB/s read throughput. Innovative solutions in the programming algorithm and circuitry produce the fastest reported 2.25MB/s programming throughput, making the device well-suited for portable code and data applications.

NOR flash technology also comes into the stringent automotive applications at the 0.13μm technology node. Paper 26.4 from Infineon presents a high-bandwidth embedded NOR flash module intended for upgradeable code storage in a -40°C to 150°C automotive environment. A fast random access time of 23.5ns, including ECC overhead, provides 2GB/s read throughput.

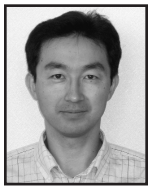
Paper 26.5 from Hitachi and Tohoku U presents a new type of MRAM technology using the spin-torque switching mechanism and sees the first megabit-level integration. This spin-tranfer torque MRAM (SPRAM) addresses the scaling problem of the high-intesity magnetic-field needed for writing in previous MRAM cells. With a reduced switching current of 200μA, this 2Mb device represents a significant improvement in MRAM design.

The final paper from Hitachi and Renesas reports a very small 0.05x0.05mm^2 chip intended for RFID-tag applications. The chip features a scalable electron-beam-written ROM for ID storage. By realizing an order-of-magnitude reduction in the chip area, this work promises to increase the convenience of electronic tagging.

26.1 A 90nm 1.8V 512Mb Diode-Switch PRAM with 266MB/s Read Throughput **8:30 AM**

K-J. Lee, Samsung Electronics, Hwasung, Korea

A 512Mb diode-switch PRAM is developed in a 90nm CMOS technology. A core configuration, read/write circuit techniques, and a charge-pump system for the diode-switch PRAM are described. Through these schemes, the PRAM achieves read throughput of 266MB/s and maximum write throughput of 4.64MB/s with a 1.8V supply.



26.2 A 512kB Embedded Phase Change Memory with 416kB/s Write Throughput at 100μA Cell Write Current **9:00 AM**

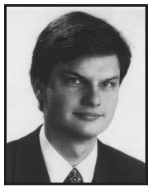
S. Hanzawa, Hitachi, Tokyo, Japan

An experimental 512kB embedded PCM uses a current-saving architecture in a 0.13μm 1.5V CMOS. The write scheme features a low-write-current resistive device and achieves 416kB/s write-throughput at 100μA cell current. A charge-transfer direct-sense scheme has a 16b parallel read access time of 9.9ns in an array drawing 280μA. A standby voltage scheme suppresses leakage current in the cell current path and increases the measured PCM cell resistance from 3 to 33MΩ.

26.3 A 65nm 1Gb 2b/Cell NOR Flash with 2.25MB/s Program Throughput and 400MB/s DDR Interface **9:30 AM**

S. Schippers, STMicroelectronics, Milan, Italy

A 1.8V 1Gb 2b/cell NOR flash memory is based on a time-domain voltage-ramp reading concept and designed in a 65nm technology. The program method, architecture and algorithm to reach 2.25MB/s programming throughput are presented. The read concept allows 70ns random access time and a 400MB/s sustained read throughput via a DDR interface.



26.4 A 0.13μm 2.125MB 23.5ns Embedded Flash with 2GB/s Read Throughput for Automotive Microcontrollers **10:15 AM**

C. Deml, Infineon Technologies, Munich, Germany

A 2.125MB embedded flash module with ECC for automotive microcontrollers is designed for a junction temperature range from -40°C to 150°C. The 23.4mm^2 module is fabricated in a 0.13μm CMOS process with non-volatile extension using a uniform cell programming NOR architecture. Careful speed optimization resulted in a 23.5ns access time and 2GB/s read throughput at a 170MHz system clock frequency.

26.5 2Mb Spin-Transfer Torque RAM (SPRAM) with Bit-by-Bit Bidirectional Current Write and Parallelizing-Direction Current Read **10:45 AM**

T. Kawahara, Hitachi, Tokyo, Japan

A 1.8V 2Mb spin-transfer torque RAM chip using a 0.2μm logic process with an MgO tunneling barrier cell demonstrates the circuit technologies for potential low-power non-volatile RAM, or universal memory. This chip features an array scheme with bit-by-bit bidirectional current write to achieve proper spin-transfer torque writing in 100ns, and parallelizing-direction current reading with a low-voltage bitline that leads to 40ns access time.

26.6 A 0.05×0.05mm^2 RFID Chip with Easily Scaled-Down ID-Memory **11:15 AM**

M. Usami, Hitachi, Tokyo, Japan

An ultra-small RFID chip uses an electron beam for writing 1T memory cells. A 90nm SOI CMOS process and double-surface electrode chip structures enable the design of 0.05×0.05mm^2 and 5μm-thick RFID chips with small, low-cost and highly-reliable 128b ID-memory. The chip is verified at a carrier frequency of 2.45GHz with measured communication distance of 300mm.